

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				2 *****
				3 *
				4 *            Zvector E6 instruction tests for VRR-b encoded:
				5 *
				6 *            E67C VSCSHP - DECIMAL SCALE AND CONVERT AND SPLIT TO HFP
				7 *
				8 *            James Wekel June 2024
				9 *****
				11 *****
				12 *
				13 *            basic instruction tests
				14 *
				15 *****
				16 *    This program tests proper functioning of the z/arch E6 VRR-b decimal
				17 *    scale adn convert and split to HFP instruction.
				18 *    Exceptions are not tested.
				19 *
				20 *    PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
				21 *    obvious coding errors.  None of the tests are thorough.  They are
				22 *    NOT designed to test all aspects of any of the instructions.
				23 *
				24 *****
				25 *
				26 *    A cross-check test is performed if the shifted packed decimal
				27 *    source can be converted to a 64-bit fixed value without overflow.
				28 *    The cross-check test converts the 64-bit fixed value to short
				29 *    float (CEGR) to compare with the high result.  The high result is
				30 *    converted back to fixed, subtracted from source 64-bit fixed, and
				31 *    converted to long float (CDGR) for create the low result.
				32 *    This low result is compared to VSCSHP low result.  An XCHECK test
				33 *    error message will be issued if there is a difference.
				34 *
				35 *****
				36 *
				37 *    *Testcase zvector-e6-18-VSCSHP: VECTOR E6 VRR-b VSCSHP instruction
				38 *    *
				39 *    *            Zvector E6 instruction tests for VRR-b encoded:
				40 *    *
				41 *    *            E67C VSCSHP - DECIMAL SCALE AND CONVERT AND SPLIT TO HFP
				42 *    *
				43 *    *            # -----
				44 *    *            #    This tests only the basic function of the instruction.
				45 *    *            #    Exceptions are NOT tested.
				46 *    *            # -----
				47 *    *
				48 *    main size        2
				49 *    numcpu           1
				50 *    sysclear
				51 *    archlvl         z/Arch
				52 *    *
				53 *    loadcore        "\$ (testpath) /zvector-e6-18-VSCSHP.core" 0x0
				54 *    *
				55 *    diag8cmd        enable        # (needed for messages to Hercules console)
				56 *    runtest 2

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
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```
57 * diagcmd disable # (reset back to default)
```

58 \*

59 \* \*Done

**60 \***

61 \*\*\*\*\*

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				63 *****
				64 * FCHECK Macro - Is a Facility Bit set?
				65 *
				66 * If the facility bit is NOT set, an message is issued and
				67 * the test is skipped.
				68 *
				69 * Fcheck uses R0, R1 and R2
				70 *
				71 * eg. FCHECK 134, 'vector-packed-decimal'
				72 *****
				73 MACRO
				74 FCHECK &BITNO, &NOTSETMSG
				75 . * &BITNO : facility bit number to check
				76 . * &NOTSETMSG : 'facility name'
				77 LCLA &FBBYTE Facility bit in Byte
				78 LCLA &FBBIT Facility bit within Byte
				79
				80 LCLA &L(8)
				81 &L(1) SetA 128, 64, 32, 16, 8, 4, 2, 1 bit positions within byte
				82
				83 &FBBYTE SETA &BITNO/8
				84 &FBBIT SETA &L((&BITNO-(&FBBYTE*8))+1)
				85 . * MNOTE 0, 'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
				86
				87 B X&SYSNDX
				88 * Fcheck data area
				89 * skip messgae
				90 SKT&SYSNDX DC C' Skipping tests: '
				91 DC C&NOTSETMSG
				92 DC C' facility (bit &BITNO) is not installed.'
				93 SKL&SYSNDX EQU *-SKT&SYSNDX
				94 * facility bits
				95 DS FD gap
				96 FB&SYSNDX DS 4FD
				97 DS FD gap
				98 *
				99 X&SYSNDX EQU *
				100 LA R0, ((X&SYSNDX- FB&SYSNDX)/8)-1
				101 STFLE FB&SYSNDX get facility bits
				102
				103 XGR R0, R0
				104 IC R0, FB&SYSNDX+&FBBYTE get fbit byte
				105 N R0, =F' &FBBIT' is bit set?
				106 BNZ XC&SYSNDX
				107 *
				108 * facility bit not set, issue message and exit
				109 *
				110 LA R0, SKL&SYSNDX message length
				111 LA R1, SKT&SYSNDX message address
				112 BAL R2, MSG
				113
				114 B EOJ
				115 XC&SYSNDX EQU *
				116 MEND



LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				137	
				138	*****
				139	* The actual "ZVE6TST" program itself...
				140	*****
				141	*
				142	* Architecture Mode: z/Arch
				143	* Register Usage:
				144	*
				145	* R0 (work)
				146	* R1-4 (work)
				147	* R5 Testing control table - current test base
				148	* R6- R7 (work)
				149	* R8 First base register
				150	* R9 Second base register
				151	* R10 Third base register
				152	* R11 E6TEST call return
				153	* R12 E6TESTS register
				154	* R13 (work)
				155	* R14 Subroutine call
				156	* R15 Secondary Subroutine call or work
				157	*
				158	*****
00000200		00000200		160	USING BEGIN, R8 FIRST Base Register
00000200		00001200		161	USING BEGIN+4096, R9 SECOND Base Register
00000200		00002200		162	USING BEGIN+8192, R10 THIRD Base Register
				163	
00000200	0580			164	BEGIN BALR R8, 0 Initalize FIRST base register
00000202	0680			165	BCTR R8, 0 Initalize FIRST base register
00000204	0680			166	BCTR R8, 0 Initalize FIRST base register
				167	
00000206	4190 8800		00000800	168	LA R9, 2048(, R8) Initalize SECOND base register
0000020A	4190 9800		00000800	169	LA R9, 2048(, R9) Initalize SECOND base register
				170	
0000020E	41A0 9800		00000800	171	LA R10, 2048(, R9) Initalize THIRD base register
00000212	41A0 A800		00000800	172	LA R10, 2048(, R10) Initalize THIRD base register
				173	
00000216	B600 838C		0000058C	174	STCTL R0, R0, CTLR0 Store CR0 to enable AFP
0000021A	9604 838D		0000058D	175	OI CTLR0+1, X' 04' Turn on AFP bit
0000021E	9602 838D		0000058D	176	OI CTLR0+1, X' 02' Turn on Vector bit
00000222	B700 838C		0000058C	177	LCTL R0, R0, CTLR0 Reload updated CR0
				178	
				179	*****
				180	* Is Vector-packed-decimal-enhancement facility 2 installed (bit 192)
				181	*****
				182	
				183	FCHECK 192, 'vector-packed-decimal-enhancement facility 2'
00000226	47F0 80C8		000002C8	184+	B X0001
				185+	*
				186+	*
					Fcheck data area skip messgae
0000022A	40404040 40404040			187+	SKT0001 DC C' Skipping tests: '
00000244	A58583A3 96996097			188+	DC C' vector-packed-decimal-enhancement facility 2'
00000270	40868183 899389A3			189+	DC C' facility (bit 192) is not installed.'
		0000006B 00000001		190+	SKL0001 EQU *- SKT0001
				191+	*
					facility bits
00000298	00000000 00000000			192+	DS FD gap







LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				243 *-----
				244 * For small (19 digit) values, cross check result
				245 * if rounding mode = 0 and conversion to 64-bit does not overflow
				246 *
				247 * R15 - RETURN
				248 *
				249 * v1,v2,v3 have result, source, scale
				250 *-----
		0000032E	00000001	251 XCHECK EQU *
				252
0000032E	E7B2 0000 0056			253 VLR V11,V2 copy source
00000334	E6AB 3019 F072			254 VSRPR V10,V11,V3,159,1 shift
0000033A	071F			255 BCR 1,R15 cc=3: overflow: ignore and return
				256
0000033C	E60A 0018 0052			257 VCVBG R0,V10,1,8 get 64-bit binary value
00000342	071F			258 BCR 1,15 cc=3: overflow: ignore and return
				259
00000344	E640 839C 2004		0000059C	260 VLLEBRZ V4,=F'0',2 zero V4 (FPR4)
0000034A	E660 839C 2004		0000059C	261 VLLEBRZ V6,=F'0',2 zero V6 (FPR6)
				262 *
				263 * convert R0 to appropriate short HFP format (high result)
				264 *
00000350	B3C4 0040			265 CEGR FPR4,R0 convert r0 to short hfp
00000354	E740 81E0 000E		000003E0	266 VST V4,XCV4
0000035A	E710 81F0 000E		000003F0	267 VST V1,XCV1
00000360	D507 81F0 81E0	000003F0	000003E0	268 CLC XCV1(8),XCV4 compare short (long) HFP
00000366	4770 8188		00000388	269 BNE XCFAIL
				270 *
				271 * build low result & compare
				272 *
0000036A	B3C8 1014			273 CGER R1,1,FPR4 convert high result back to fixed
0000036E	B9E9 1020			274 SGRK R2,R0,R1 split ie. subtract high result
00000372	B3C5 0042			275 CDGR FPR4,R2 convert r2 to long hfp
00000376	E740 81E0 000E		000003E0	276 VST V4,XCV4
0000037C	D507 81F8 81E0	000003F8	000003E0	277 CLC XCV1+8(8),XCV4 compare low result long HFP
00000382	4770 8188		00000388	278 BNE XCFAIL
00000386	07FF			279 BR R15 0k, exit
				280
00000388				281 * xcheck failed message
00000388	4820 5004		00000004	282 XCFAIL DS OH
0000038C	4E20 8EBB		000010BB	283 LH R2,TNUM get test number and convert
00000390	D211 8EA5 8E8F	000010A5	0000108F	284 CVD R2,DECNUM
00000396	DE11 8EA5 8EBB	000010A5	000010BB	285 MWC PRT3,EDIT
0000039C	D202 8E55 8EB2	00001055	000010B2	286 ED PRT3,DECNUM
				287 MWC XCPTNUM(3),PRT3+13 fill in message with test #
				288
000003A2	D207 8E77 500C	00001077	0000000C	289 MWC XCPNAME,OPNAME fill in message with instruction
				290
000003A8	B982 0022			291 XGR R2,R2 get scale as U8
000003AC	4320 5007		00000007	292 IC R2,SCALE and convert
000003B0	4E20 8EBB		000010BB	293 CVD R2,DECNUM
000003B4	D211 8EA5 8E8F	000010A5	0000108F	294 MWC PRT3,EDIT
000003BA	DE11 8EA5 8EBB	000010A5	000010BB	295 ED PRT3,DECNUM
000003C0	D202 8E8B 8EB2	0000108B	000010B2	296 MWC XCPSCALE(3),PRT3+13 fill in message with scale field
				297
000003C6	50F0 8200		00000400	298 ST R15,XCR15 save r15





LOC	OBJECT CODE			ADDR1	ADDR2	STMT	
						312	*****
						313	* result not as expected:
						314	* issue message with test number, instruction under test
						315	* and instruction i3
						316	*****
				00000408	00000001	317	FAILMSG EQU *
00000408	4820	5004			00000004	318	LH R2, TNUM get test number and convert
0000040C	4E20	8EBB			000010BB	319	CVD R2, DECNUM
00000410	D211	8EA5 8E8F		000010A5	0000108F	320	MVC PRT3, EDIT
00000416	DE11	8EA5 8EBB		000010A5	000010BB	321	ED PRT3, DECNUM
0000041C	D202	8E15 8EB2		00001015	000010B2	322	MVC PRTNUM(3), PRT3+13 fill in message with test #
						323	
00000422	D207	8E30 500C		00001030	0000000C	324	MVC PRTNAME, OPNAME fill in message with instruction
						325	*
00000428	B982	0022				326	XGR R2, R2
0000042C	4320	5007			00000007	327	IC R2, SCALE get scale and convert
00000430	4E20	8EBB			000010BB	328	CVD R2, DECNUM
00000434	D211	8EA5 8E8F		000010A5	0000108F	329	MVC PRT3, EDIT
0000043A	DE11	8EA5 8EBB		000010A5	000010BB	330	ED PRT3, DECNUM
00000440	D202	8E44 8EB2		00001044	000010B2	331	MVC PRTSCALE(3), PRT3+13 fill in message with scale
						332	
00000446	4100	0040			00000040	333	LA R0, PRTLNG message length
0000044A	4110	8E08			00001008	334	LA R1, PRTLNE messagfe address
0000044E	45F0	8270			00000470	335	BAL R15, RPTERROR
						337	*****
						338	* continue after a failed test
						339	*****
				00000452	00000001	340	FAILCONT EQU *
00000452	5800	83A0			000005A0	341	L R0, =F' 1' set failed test indicator
00000456	5000	8E00			00001000	342	ST R0, FAILED
						343	
0000045A	41C0	C004			00000004	344	LA R12, 4(0, R12) next test address
0000045E	47F0	80F4			000002F4	345	B NEXTE6
						347	*****
						348	* end of testing; set ending psw
						349	*****
				00000462	00000001	350	ENDTEST EQU *
00000462	5810	8E00			00001000	351	L R1, FAILED did a test fail?
00000466	1211					352	LTR R1, R1
00000468	4780	8370			00000570	353	BZ E0J No, exit
0000046C	47F0	8388			00000588	354	B FAILTEST Yes, exit with BAD PSW
						355	





LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				420 *****
				421 *            Normal completion or Abnormal termination PSWs
				422 *****
00000560	00020001 80000000			424 EOJPSW    DC        0D' 0' , X' 0002000180000000' , AD(0)
00000570	B2B2 8360		00000560	426 EOJ            LPSWE EOJPSW                    Normal completion
00000578	00020001 80000000			428 FAILPSW    DC        0D' 0' , X' 0002000180000000' , AD(X' BAD' )
00000588	B2B2 8378		00000578	430 FAILTEST LPSWE FAILPSW                    Abnormal termination
				432 *****
				433 *            Working Storage
				434 *****
0000058C	00000000			436 CTLR0        DS        F                    CRO
00000590	00000000			437                DS        F
00000594				439
00000594	00000080			440                LTORG ,                    Literals pool
00000598	00001974			441                    =F' 128'
0000059C	00000000			442                    =A(E6TESTS)
000005A0	00000001			443                    =F' 0'
000005A4	0000			444                    =F' 1'
000005A6	005F			445                    =H' 0'
				446                    =AL2(L' MSGMSG)
				447
				448 *            some constants
				449
	00000400	00000001		450 K            EQU        1024                    One KB
	00001000	00000001		451 PAGE        EQU        (4*K)                    Size of one page
	00010000	00000001		452 K64        EQU        (64*K)                    64 KB
	00100000	00000001		453 MB        EQU        (K*K)                    1 MB
				454
	AABBCCDD	00000001		455 REG2PATT EQU        X' AABBCCDD'            Polluted Register pattern
	000000DD	00000001		456 REG2LOW EQU                    X' DD'            (last byte above)







LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				520	*****
				521	*            E6TEST DSECT
				522	*****
				524	E6TEST    DSECT ,
00000000	00000000			525	TSUB       DC    A(0)            pointer to test
00000004	0000			526	TNUM       DC    H' 00'            Test Number
00000006	00			527	DC    X' 00'
00000007	00			528	SCALE       DC    HL1' 00'            scale used
00000008	00000000			529	V2ADDR      DC    A(0)            address of v2: 16-byte packed decimal
0000000C	40404040	40404040		530	OPNAME      DC    CL8' '            E6 name
00000014	00000000			531	RELEN       DC    A(0)            result length
00000018	00000000			532	READDR      DC    A(0)            expected result address
				533	
				534	**
				535	*            test routine will be here (from VRR-b macro)
				537	ZVE6TST    CSECT ,
0000112C		00000000	000019DB	538	DS        0F
				540	*****
				541	*            Macros to help build test tables
				542	*****
				544	*
				545	*    macro to generate individual test
				546	*
				547	MACRO
				548	VRR_B &INST, &SCALE
				549	. *                                    &INST - VRR-b instruction under test
				550	
				551	GBLA    &TNUM
				552	&TNUM    SETA    &TNUM+1
				553	
				554	DS       0FD
				555	USING    *, R5            base for test data and test routine
				556	
				557	T&TNUM    DC    A(X&TNUM)            address of test routine
				558	DC    H' &TNUM            test number
				559	DC    X' 00'
				560	V3_&TNUM DC    HL1' &SCALE'            scale
				561	V2_&TNUM DC    A(RE&TNUM+16)            address of v2: 16-byte packed decimal
				562	DC    CL8' &INST'            instruction name
				563	DC    A(16)            result length
				564	DC    A(RE&TNUM)            address of expected result
				565	. *
				566	*
				567	X&TNUM    DS    0F
				568	VL        V1, V1FUDGE            fudge V1
				569	
				570	LGF       R2, V2_&TNUM            get v2



LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				606 *****	
				607 * E6 VRR-b tests	
				608 *****	
				609 PRINT DATA	
				610 *	
				611 * E67C VSCSHP - DECIMAL SCALE AND CONVERT AND SPLIT TO HFP	
				612 *	
				613 *-----	
				614 * VSCSHP - DECIMAL SCALE AND CONVERT AND SPLIT TO HFP	
				615 *-----	
				616 * VRR-b instruction	
				617 * followed by	
				618 * followed by	
				619 * v1 - 16 byte expected result	
				620 * v2 - 16 byte zoned decimal (operand)	
				621 *-----	
				622 * NO Shift/Scale	
				623 *-----	
				624	
				625 * +0	
00001130				626 VRR_B VSCSHP, 0	
00001130		00001130		627+ DS OFD	
00001130	0000114C			628+ USING *, R5	base for test data and test routine
00001134	0001			629+T1 DC A(X1)	address of test routine
00001136	00			630+ DC H' 1'	test number
00001137	00			631+ DC X' 00'	
00001138	0000117C			632+V3_1 DC HL1' 0'	scale
0000113C	E5E2C3E2 C8D74040			633+V2_1 DC A(RE1+16)	address of v2: 16-byte packed decimal
00001144	00000010			634+ DC CL8' VSCSHP'	instruction name
00001148	0000116C			635+ DC A(16)	result length
				636+ DC A(RE1)	address of expected result
				637+*	
0000114C				638+X1 DS OF	
0000114C	E710 8EFC 0006	000010FC		639+ VL V1, V1FUDGE	fudge V1
00001152	E320 5008 0014	00001138		640+ LGF R2, V2_1	get v2
00001158	E722 0000 0006	00000000		641+ VL V2, 0(R2)	
0000115E	E730 5007 7000	00001137		642+ VLEB V3, V3_1, 7	get v3 scale
00001164	E612 3000 007C			643+ VSCSHP V1, V2, V3	test instruction
0000116A	07FB			644+ BR R11	return
0000116C				645+RE1 DS OF	expected 16 byte result
0000116C				646+ DROP R5	
0000116C	00000000 00000000			647 DC XL16' 00000000000000000000000000000000'	
00001174	00000000 00000000				
0000117C	00000000 00000000			648 DC XL16' 00000000000000000000000000000000C'	
00001184	00000000 0000000C				
				649 * -0	
				650	
00001190				651+ VRR_B VSCSHP, 0	
00001190		00001190		652+ DS OFD	
00001190	000011AC			653+T2 USING *, R5	base for test data and test routine
00001194	0002			654+ DC A(X2)	address of test routine
00001196	00			655+ DC H' 2'	test number
00001197	00			656+V3_2 DC X' 00'	
00001198	000011DC			657+V2_2 DC HL1' 0'	scale
0000119C	E5E2C3E2 C8D74040			658+ DC A(RE2+16)	address of v2: 16-byte packed decimal
000011A4	00000010			659+ DC CL8' VSCSHP'	instruction name
				DC A(16)	result length

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000011A8	000011CC			660+ 661+*	DC	A(RE2)	address of expected result
000011AC				662+X2	DS	OF	
000011AC	E710 8EFC 0006		000010FC	663+	VL	V1, V1FUDGE	fudge V1
000011B2	E320 5008 0014		00001198	664+	LGF	R2, V2_2	get v2
000011B8	E722 0000 0006		00000000	665+	VL	V2, 0(R2)	
000011BE	E730 5007 7000		00001197	666+	VLEB	V3, V3_2, 7	get v3 scale
000011C4	E612 3000 007C			667+	VSCSHP	V1, V2, V3	test instruction
000011CA	07FB			668+	BR	R11	return
000011CC				669+RE2	DS	OF	expected 16 byte result
000011CC				670+	DROP	R5	
000011CC	00000000 00000000			671	DC	XL16' 00000000000000000000000000000000'	
000011D4	00000000 00000000						
000011DC	00000000 00000000			672	DC	XL16' 00000000000000000000000000000000D'	
000011E4	00000000 0000000D						
				673 * +1			
				674	VRR_B	VSCSHP, 0	
000011F0				675+	DS	OFD	
000011F0		000011F0		676+	USING	*, R5	base for test data and test routine
000011F0	0000120C			677+T3	DC	A(X3)	address of test routine
000011F4	0003			678+	DC	H' 3'	test number
000011F6	00			679+	DC	X' 00'	
000011F7	00			680+V3_3	DC	HL1' 0'	scale
000011F8	0000123C			681+V2_3	DC	A(RE3+16)	address of v2: 16-byte packed decimal
000011FC	E5E2C3E2 C8D74040			682+	DC	CL8' VSCSHP'	instruction name
00001204	00000010			683+	DC	A(16)	result length
00001208	0000122C			684+	DC	A(RE3)	address of expected result
				685+*			
0000120C				686+X3	DS	OF	
0000120C	E710 8EFC 0006		000010FC	687+	VL	V1, V1FUDGE	fudge V1
00001212	E320 5008 0014		000011F8	688+	LGF	R2, V2_3	get v2
00001218	E722 0000 0006		00000000	689+	VL	V2, 0(R2)	
0000121E	E730 5007 7000		000011F7	690+	VLEB	V3, V3_3, 7	get v3 scale
00001224	E612 3000 007C			691+	VSCSHP	V1, V2, V3	test instruction
0000122A	07FB			692+	BR	R11	return
0000122C				693+RE3	DS	OF	expected 16 byte result
0000122C				694+	DROP	R5	
0000122C	41100000 00000000			695	DC	XL16' 41100000000000000000000000000000'	
00001234	00000000 00000000						
0000123C	00000000 00000000			696	DC	XL16' 000000000000000000000000000000001C'	
00001244	00000000 0000001C						
				697 * -1			
				698	VRR_B	VSCSHP, 0	
00001250				699+	DS	OFD	
00001250		00001250		700+	USING	*, R5	base for test data and test routine
00001250	0000126C			701+T4	DC	A(X4)	address of test routine
00001254	0004			702+	DC	H' 4'	test number
00001256	00			703+	DC	X' 00'	
00001257	00			704+V3_4	DC	HL1' 0'	scale
00001258	0000129C			705+V2_4	DC	A(RE4+16)	address of v2: 16-byte packed decimal
0000125C	E5E2C3E2 C8D74040			706+	DC	CL8' VSCSHP'	instruction name
00001264	00000010			707+	DC	A(16)	result length
00001268	0000128C			708+	DC	A(RE4)	address of expected result
				709+*			
0000126C				710+X4	DS	OF	
0000126C	E710 8EFC 0006		000010FC	711+	VL	V1, V1FUDGE	fudge V1

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001272	E320 5008 0014		00001258	712+	LGF	R2, V2_4	get v2
00001278	E722 0000 0006		00000000	713+	VL	V2, 0(R2)	
0000127E	E730 5007 7000		00001257	714+	VLEB	V3, V3_4, 7	get v3 scale
00001284	E612 3000 007C			715+	VSCSHP	V1, V2, V3	test instruction
0000128A	07FB			716+	BR	R11	return
0000128C				717+RE4	DS	0F	expected 16 byte result
0000128C				718+	DROP	R5	
0000128C	C1100000 00000000			719	DC	XL16' C110000000000000000000000000000000'	
00001294	00000000 00000000						
0000129C	00000000 00000000			720	DC	XL16' 0000000000000000000000000000000001D'	
000012A4	00000000 0000001D						
				721			
				722	*	- 36650385409	
				723	VRR_B	VSCSHP, 0	
000012B0				724+	DS	0FD	
000012B0		000012B0		725+	USING	*, R5	base for test data and test routine
000012B0	000012CC			726+T5	DC	A(X5)	address of test routine
000012B4	0005			727+	DC	H' 5'	test number
000012B6	00			728+	DC	X' 00'	
000012B7	00			729+V3_5	DC	HL1' 0'	scale
000012B8	000012FC			730+V2_5	DC	A(RE5+16)	address of v2: 16-byte packed decimal
000012BC	E5E2C3E2 C8D74040			731+	DC	CL8' VSCSHP'	instruction name
000012C4	00000010			732+	DC	A(16)	result length
000012C8	000012EC			733+	DC	A(RE5)	address of expected result
				734+*			
000012CC				735+X5	DS	0F	
000012CC	E710 8EFC 0006		000010FC	736+	VL	V1, V1FUDGE	fudge V1
000012D2	E320 5008 0014		000012B8	737+	LGF	R2, V2_5	get v2
000012D8	E722 0000 0006		00000000	738+	VL	V2, 0(R2)	
000012DE	E730 5007 7000		000012B7	739+	VLEB	V3, V3_5, 7	get v3 scale
000012E4	E612 3000 007C			740+	VSCSHP	V1, V2, V3	test instruction
000012EA	07FB			741+	BR	R11	return
000012EC				742+RE5	DS	0F	expected 16 byte result
000012EC				743+	DROP	R5	
000012EC	C9888888 00000000			744	DC	XL16' C9888888000000000C110000000000000'	
000012F4	C1100000 00000000						
000012FC	00000000 00000000			745	DC	XL16' 000000000000000000000036650385409D'	
00001304	00003665 0385409D						
				746			
				747	*	+9000000000000000001	
				748	VRR_B	VSCSHP, 0	
00001310				749+	DS	0FD	
00001310		00001310		750+	USING	*, R5	base for test data and test routine
00001310	0000132C			751+T6	DC	A(X6)	address of test routine
00001314	0006			752+	DC	H' 6'	test number
00001316	00			753+	DC	X' 00'	
00001317	00			754+V3_6	DC	HL1' 0'	scale
00001318	0000135C			755+V2_6	DC	A(RE6+16)	address of v2: 16-byte packed decimal
0000131C	E5E2C3E2 C8D74040			756+	DC	CL8' VSCSHP'	instruction name
00001324	00000010			757+	DC	A(16)	result length
00001328	0000134C			758+	DC	A(RE6)	address of expected result
				759+*			
0000132C				760+X6	DS	0F	
0000132C	E710 8EFC 0006		000010FC	761+	VL	V1, V1FUDGE	fudge V1
00001332	E320 5008 0014		00001318	762+	LGF	R2, V2_6	get v2
00001338	E722 0000 0006		00000000	763+	VL	V2, 0(R2)	



LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
0000133E	E730 5007 7000		00001317	764+	VLEB V3, V3_6, 7	get v3 scale
00001344	E612 3000 007C			765+	VSCSHP V1, V2, V3	test instruction
0000134A	07FB			766+	BR R11	return
0000134C				767+RE6	DS 0F	expected 16 byte result
0000134C				768+	DROP R5	
0000134C	4E1FF973 00000000			769	DC XL16' 4E1FF97300000000048CAFA8001000000'	
00001354	48CAFA80 01000000					
0000135C	00000000 00000009			770	DC XL16' 0000000000000009000000000000001C'	
00001364	00000000 0000001C					
				771		
				772 *	- 9223372036854775808	
				773	VRR_B VSCSHP, 0	
00001370				774+	DS 0FD	
00001370		00001370		775+	USING *, R5	base for test data and test routine
00001370	0000138C			776+T7	DC A(X7)	address of test routine
00001374	0007			777+	DC H' 7'	test number
00001376	00			778+	DC X' 00'	
00001377	00			779+V3_7	DC HL1' 0'	scale
00001378	000013BC			780+V2_7	DC A(RE7+16)	address of v2: 16-byte packed decimal
0000137C	E5E2C3E2 C8D74040			781+	DC CL8' VSCSHP'	instruction name
00001384	00000010			782+	DC A(16)	result length
00001388	000013AC			783+	DC A(RE7)	address of expected result
				784+*		
0000138C				785+X7	DS 0F	
0000138C	E710 8EFC 0006		000010FC	786+	VL V1, V1FUDGE	fudge V1
00001392	E320 5008 0014		00001378	787+	LGF R2, V2_7	get v2
00001398	E722 0000 0006		00000000	788+	VL V2, 0(R2)	
0000139E	E730 5007 7000		00001377	789+	VLEB V3, V3_7, 7	get v3 scale
000013A4	E612 3000 007C			790+	VSCSHP V1, V2, V3	test instruction
000013AA	07FB			791+	BR R11	return
000013AC				792+RE7	DS 0F	expected 16 byte result
000013AC				793+	DROP R5	
000013AC	D0800000 00000000			794	DC XL16' D0800000000000000000000000000000'	
000013B4	00000000 00000000					
000013BC	00000000 00009223			795	DC XL16' 00000000000009223372036854775808D'	
000013C4	37203685 4775808D					
				796		
				797 *	9223372036854775807	
				798	VRR_B VSCSHP, 0	
000013D0				799+	DS 0FD	
000013D0		000013D0		800+	USING *, R5	base for test data and test routine
000013D0	000013EC			801+T8	DC A(X8)	address of test routine
000013D4	0008			802+	DC H' 8'	test number
000013D6	00			803+	DC X' 00'	
000013D7	00			804+V3_8	DC HL1' 0'	scale
000013D8	0000141C			805+V2_8	DC A(RE8+16)	address of v2: 16-byte packed decimal
000013DC	E5E2C3E2 C8D74040			806+	DC CL8' VSCSHP'	instruction name
000013E4	00000010			807+	DC A(16)	result length
000013E8	0000140C			808+	DC A(RE8)	address of expected result
				809+*		
000013EC				810+X8	DS 0F	
000013EC	E710 8EFC 0006		000010FC	811+	VL V1, V1FUDGE	fudge V1
000013F2	E320 5008 0014		000013D8	812+	LGF R2, V2_8	get v2
000013F8	E722 0000 0006		00000000	813+	VL V2, 0(R2)	
000013FE	E730 5007 7000		000013D7	814+	VLEB V3, V3_8, 7	get v3 scale
00001404	E612 3000 007C			815+	VSCSHP V1, V2, V3	test instruction

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
0000140A	07FB			816+	BR R11	return
0000140C				817+RE8	DS 0F	expected 16 byte result
0000140C				818+	DROP R5	
0000140C	507FFFFFFF 00000000			819	DC XL16' 507FFFFFFF000000004AFFFFFFFFFFFF0000'	
00001414	4AFFFFFF FFFF0000					
0000141C	00000000 00009223			820	DC XL16' 00000000000009223372036854775807C'	
00001424	37203685 4775807C					
				821		
				822 *	18446744073709551615	
				823	VRR_B VSCSHP, 0	
00001430				824+	DS 0FD	
00001430		00001430		825+	USING *, R5	base for test data and test routine
00001430	0000144C			826+T9	DC A(X9)	address of test routine
00001434	0009			827+	DC H' 9'	test number
00001436	00			828+	DC X' 00'	
00001437	00			829+V3_9	DC HL1' 0'	scale
00001438	0000147C			830+V2_9	DC A(RE9+16)	address of v2: 16-byte packed decimal
0000143C	E5E2C3E2 C8D74040			831+	DC CL8' VSCSHP'	instruction name
00001444	00000010			832+	DC A(16)	result length
00001448	0000146C			833+	DC A(RE9)	address of expected result
				834+*		
0000144C				835+X9	DS 0F	
0000144C	E710 8EFC 0006		000010FC	836+	VL V1, V1FUDGE	fudge V1
00001452	E320 5008 0014		00001438	837+	LGF R2, V2_9	get v2
00001458	E722 0000 0006		00000000	838+	VL V2, 0(R2)	
0000145E	E730 5007 7000		00001437	839+	VLEB V3, V3_9, 7	get v3 scale
00001464	E612 3000 007C			840+	VSCSHP V1, V2, V3	test instruction
0000146A	07FB			841+	BR R11	return
0000146C				842+RE9	DS 0F	expected 16 byte result
0000146C				843+	DROP R5	
0000146C	50FFFFFF 00000000			844	DC XL16' 50FFFFFF000000004AFFFFFFFFFFFF0000'	
00001474	4AFFFFFF FFFF0000					
0000147C	00000000 00018446			845	DC XL16' 00000000000018446744073709551615C'	
00001484	74407370 9551615C					
				846		
				847 *	90090000000018446744073709551615	
				848	VRR_B VSCSHP, 0	
00001490				849+	DS 0FD	
00001490		00001490		850+	USING *, R5	base for test data and test routine
00001490	000014AC			851+T10	DC A(X10)	address of test routine
00001494	000A			852+	DC H' 10'	test number
00001496	00			853+	DC X' 00'	
00001497	00			854+V3_10	DC HL1' 0'	scale
00001498	000014DC			855+V2_10	DC A(RE10+16)	address of v2: 16-byte packed decimal
0000149C	E5E2C3E2 C8D74040			856+	DC CL8' VSCSHP'	instruction name
000014A4	00000010			857+	DC A(16)	result length
000014A8	000014CC			858+	DC A(RE10)	address of expected result
				859+*		
000014AC				860+X10	DS 0F	
000014AC	E710 8EFC 0006		000010FC	861+	VL V1, V1FUDGE	fudge V1
000014B2	E320 5008 0014		00001498	862+	LGF R2, V2_10	get v2
000014B8	E722 0000 0006		00000000	863+	VL V2, 0(R2)	
000014BE	E730 5007 7000		00001497	864+	VLEB V3, V3_10, 7	get v3 scale
000014C4	E612 3000 007C			865+	VSCSHP V1, V2, V3	test instruction
000014CA	07FB			866+	BR R11	return
000014CC				867+RE10	DS 0F	expected 16 byte result



LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
000014CC				868+	DROP R5	
000014CC	5A71B5A6 00000000			869	DC	XL16' 5A71B5A60000000005423751870DF6067'
000014D4	54237518 70DF6067					
000014DC	90090000 00018446			870	DC	XL16' 90090000000018446744073709551615C'
000014E4	74407370 9551615C					
				871		
				872 *	9999999990018446744073709551615	
				873	VRR_B VSCSHP, 0	
000014F0				874+	DS	OFD
000014F0		000014F0		875+	USING *, R5	base for test data and test routine
000014F0	0000150C			876+T11	DC	A(X11)
000014F4	000B			877+	DC	H' 11'
000014F6	00			878+	DC	X' 00'
000014F7	00			879+V3_11	DC	HL1' 0'
000014F8	0000153C			880+V2_11	DC	A(RE11+16)
000014FC	E5E2C3E2 C8D74040			881+	DC	CL8' VSCSHP'
00001504	00000010			882+	DC	A(16)
00001508	0000152C			883+	DC	A(RE11)
				884+*		address of expected result
0000150C				885+X11	DS	OF
0000150C	E710 8EFC 0006		000010FC	886+	VL	V1, V1FUDGE
00001512	E320 5008 0014		000014F8	887+	LGF	R2, V2_11
00001518	E722 0000 0006		00000000	888+	VL	V2, 0(R2)
0000151E	E730 5007 7000		000014F7	889+	VLEB	V3, V3_11, 7
00001524	E612 3000 007C			890+	VSCSHP	V1, V2, V3
0000152A	07FB			891+	BR	R11
0000152C				892+RE11	DS	OF
0000152C				893+	DROP	R5
0000152C	5A7E37BE 00000000			894	DC	XL16' 5A7E37BE000000000541E05A6B0816BCD'
00001534	541E05A6 B0816BCD					
0000153C	99999999 90018446			895	DC	XL16' 9999999990018446744073709551615C'
00001544	74407370 9551615C					
				896		
				897 *	-----	
				898 *	With Shift/Scale	
				899 *	-----	
				900		
				901 *	+0	
				902	VRR_B VSCSHP, 1	
00001550				903+	DS	OFD
00001550		00001550		904+	USING *, R5	base for test data and test routine
00001550	0000156C			905+T12	DC	A(X12)
00001554	000C			906+	DC	H' 12'
00001556	00			907+	DC	X' 00'
00001557	01			908+V3_12	DC	HL1' 1'
00001558	0000159C			909+V2_12	DC	A(RE12+16)
0000155C	E5E2C3E2 C8D74040			910+	DC	CL8' VSCSHP'
00001564	00000010			911+	DC	A(16)
00001568	0000158C			912+	DC	A(RE12)
				913+*		address of expected result
0000156C				914+X12	DS	OF
0000156C	E710 8EFC 0006		000010FC	915+	VL	V1, V1FUDGE
00001572	E320 5008 0014		00001558	916+	LGF	R2, V2_12
00001578	E722 0000 0006		00000000	917+	VL	V2, 0(R2)
0000157E	E730 5007 7000		00001557	918+	VLEB	V3, V3_12, 7
00001584	E612 3000 007C			919+	VSCSHP	V1, V2, V3
						test instruction

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000158A	07FB			920+	BR	R11	return
0000158C				921+RE12	DS	0F	expected 16 byte result
0000158C				922+	DROP	R5	
0000158C	00000000 00000000			923	DC	XL16'	00000000000000000000000000000000'
00001594	00000000 00000000						
0000159C	00000000 00000000			924	DC	XL16'	00000000000000000000000000000000C'
000015A4	00000000 0000000C						
				925 * -0			
				926	VRR_B	VSCSHP, 1	
000015B0				927+	DS	0FD	
000015B0		000015B0		928+	USING	*, R5	base for test data and test routine
000015B0	000015CC			929+T13	DC	A(X13)	address of test routine
000015B4	000D			930+	DC	H' 13'	test number
000015B6	00			931+	DC	X' 00'	
000015B7	01			932+V3_13	DC	HL1' 1'	scale
000015B8	000015FC			933+V2_13	DC	A(RE13+16)	address of v2: 16-byte packed decimal
000015BC	E5E2C3E2 C8D74040			934+	DC	CL8' VSCSHP'	instruction name
000015C4	00000010			935+	DC	A(16)	result length
000015C8	000015EC			936+	DC	A(RE13)	address of expected result
				937+*			
000015CC				938+X13	DS	0F	
000015CC	E710 8EFC 0006		000010FC	939+	VL	V1, V1FUDGE	fudge V1
000015D2	E320 5008 0014		000015B8	940+	LGF	R2, V2_13	get v2
000015D8	E722 0000 0006		00000000	941+	VL	V2, 0(R2)	
000015DE	E730 5007 7000		000015B7	942+	VLEB	V3, V3_13, 7	get v3 scale
000015E4	E612 3000 007C			943+	VSCSHP	V1, V2, V3	test instruction
000015EA	07FB			944+	BR	R11	return
000015EC				945+RE13	DS	0F	expected 16 byte result
000015EC				946+	DROP	R5	
000015EC	00000000 00000000			947	DC	XL16'	00000000000000000000000000000000'
000015F4	00000000 00000000						
000015FC	00000000 00000000			948	DC	XL16'	00000000000000000000000000000000D'
00001604	00000000 0000000D						
				949 * +1			
				950	VRR_B	VSCSHP, 1	
00001610				951+	DS	0FD	
00001610		00001610		952+	USING	*, R5	base for test data and test routine
00001610	0000162C			953+T14	DC	A(X14)	address of test routine
00001614	000E			954+	DC	H' 14'	test number
00001616	00			955+	DC	X' 00'	
00001617	01			956+V3_14	DC	HL1' 1'	scale
00001618	0000165C			957+V2_14	DC	A(RE14+16)	address of v2: 16-byte packed decimal
0000161C	E5E2C3E2 C8D74040			958+	DC	CL8' VSCSHP'	instruction name
00001624	00000010			959+	DC	A(16)	result length
00001628	0000164C			960+	DC	A(RE14)	address of expected result
				961+*			
0000162C				962+X14	DS	0F	
0000162C	E710 8EFC 0006		000010FC	963+	VL	V1, V1FUDGE	fudge V1
00001632	E320 5008 0014		00001618	964+	LGF	R2, V2_14	get v2
00001638	E722 0000 0006		00000000	965+	VL	V2, 0(R2)	
0000163E	E730 5007 7000		00001617	966+	VLEB	V3, V3_14, 7	get v3 scale
00001644	E612 3000 007C			967+	VSCSHP	V1, V2, V3	test instruction
0000164A	07FB			968+	BR	R11	return
0000164C				969+RE14	DS	0F	expected 16 byte result
0000164C				970+	DROP	R5	
0000164C	41A00000 00000000			971	DC	XL16'	41A00000000000000000000000000000'



LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				1022	
				1023 * +900000000000000001	
00001730				1024	VRR_B VSCSHP, 2
00001730		00001730		1025+	DS OFD
00001730	0000174C			1026+	USING *, R5
00001734	0011			1027+T17	DC A(X17)
00001736	00			1028+	DC H' 17'
00001737	02			1029+	DC X' 00'
00001738	0000177C			1030+V3_17	DC HL1' 2'
0000173C	E5E2C3E2 C8D74040			1031+V2_17	DC A(RE17+16)
00001744	00000010			1032+	DC CL8' VSCSHP'
00001748	0000176C			1033+	DC A(16)
				1034+	DC A(RE17)
				1035+*	
0000174C				1036+X17	DS OF
0000174C	E710 8EFC 0006		000010FC	1037+	VL V1, V1FUDGE
00001752	E320 5008 0014		00001738	1038+	LGF R2, V2_17
00001758	E722 0000 0006		00000000	1039+	VL V2, 0(R2)
0000175E	E730 5007 7000		00001737	1040+	VLEB V3, V3_17, 7
00001764	E612 3000 007C			1041+	VSCSHP V1, V2, V3
0000176A	07FB			1042+	BR R11
0000176C				1043+RE17	DS OF
0000176C				1044+	DROP R5
0000176C	4FC7D713 00000000			1045	DC XL16' 4FC7D71300000000049B49DA006400000'
00001774	49B49DA0 06400000				
0000177C	00000000 00000009			1046	DC XL16' 000000000000000090000000000000001C'
00001784	00000000 0000001C				
				1047	
				1048 * -9223372036854775808	
00001790				1049	VRR_B VSCSHP, 2
00001790		00001790		1050+	DS OFD
00001790	000017AC			1051+	USING *, R5
00001794	0012			1052+T18	DC A(X18)
00001796	00			1053+	DC H' 18'
00001797	02			1054+	DC X' 00'
00001798	000017DC			1055+V3_18	DC HL1' 2'
0000179C	E5E2C3E2 C8D74040			1056+V2_18	DC A(RE18+16)
000017A4	00000010			1057+	DC CL8' VSCSHP'
000017A8	000017CC			1058+	DC A(16)
				1059+	DC A(RE18)
				1060+*	
000017AC				1061+X18	DS OF
000017AC	E710 8EFC 0006		000010FC	1062+	VL V1, V1FUDGE
000017B2	E320 5008 0014		00001798	1063+	LGF R2, V2_18
000017B8	E722 0000 0006		00000000	1064+	VL V2, 0(R2)
000017BE	E730 5007 7000		00001797	1065+	VLEB V3, V3_18, 7
000017C4	E612 3000 007C			1066+	VSCSHP V1, V2, V3
000017CA	07FB			1067+	BR R11
000017CC				1068+RE18	DS OF
000017CC				1069+	DROP R5
000017CC	D2320000 00000000			1070	DC XL16' D2320000000000000000000000000000'
000017D4	00000000 00000000				
000017DC	00000000 00009223			1071	DC XL16' 00000000000009223372036854775808D'
000017E4	37203685 4775808D				
				1072	
				1073 * 9223372036854775807	



LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
000017F0				1074	VRR_B VSCSHP, 2	
000017F0				1075+	DS OFD	
000017F0		000017F0		1076+	USING *, R5	base for test data and test routine
000017F0	0000180C			1077+T19	DC A(X19)	address of test routine
000017F4	0013			1078+	DC H' 19'	test number
000017F6	00			1079+	DC X' 00'	
000017F7	02			1080+V3_19	DC HL1' 2'	scale
000017F8	0000183C			1081+V2_19	DC A(RE19+16)	address of v2: 16-byte packed decimal
000017FC	E5E2C3E2 C8D74040			1082+	DC CL8' VSCSHP'	instruction name
00001804	00000010			1083+	DC A(16)	result length
00001808	0000182C			1084+	DC A(RE19)	address of expected result
				1085+*		
0000180C				1086+X19	DS OF	
0000180C	E710 8EFC 0006		000010FC	1087+	VL V1, V1FUDGE	fudge V1
00001812	E320 5008 0014		000017F8	1088+	LGF R2, V2_19	get v2
00001818	E722 0000 0006		00000000	1089+	VL V2, 0(R2)	
0000181E	E730 5007 7000		000017F7	1090+	VLEB V3, V3_19, 7	get v3 scale
00001824	E612 3000 007C			1091+	VSCSHP V1, V2, V3	test instruction
0000182A	07FB			1092+	BR R11	return
0000182C				1093+RE19	DS OF	expected 16 byte result
0000182C				1094+	DROP R5	
0000182C	5231FFFF 00000000			1095	DC XL16' 5231FFFF000000004CFFFFFFFFFFFF9C00'	
00001834	4CFFFFFFFF FFFF9C00					
0000183C	00000000 00009223			1096	DC XL16' 0000000000009223372036854775807C'	
00001844	37203685 4775807C					
				1097		
				1098 * 18446744073709551615		
				1099	VRR_B VSCSHP, 2	
00001850				1100+	DS OFD	
00001850		00001850		1101+	USING *, R5	base for test data and test routine
00001850	0000186C			1102+T20	DC A(X20)	address of test routine
00001854	0014			1103+	DC H' 20'	test number
00001856	00			1104+	DC X' 00'	
00001857	02			1105+V3_20	DC HL1' 2'	scale
00001858	0000189C			1106+V2_20	DC A(RE20+16)	address of v2: 16-byte packed decimal
0000185C	E5E2C3E2 C8D74040			1107+	DC CL8' VSCSHP'	instruction name
00001864	00000010			1108+	DC A(16)	result length
00001868	0000188C			1109+	DC A(RE20)	address of expected result
				1110+*		
0000186C				1111+X20	DS OF	
0000186C	E710 8EFC 0006		000010FC	1112+	VL V1, V1FUDGE	fudge V1
00001872	E320 5008 0014		00001858	1113+	LGF R2, V2_20	get v2
00001878	E722 0000 0006		00000000	1114+	VL V2, 0(R2)	
0000187E	E730 5007 7000		00001857	1115+	VLEB V3, V3_20, 7	get v3 scale
00001884	E612 3000 007C			1116+	VSCSHP V1, V2, V3	test instruction
0000188A	07FB			1117+	BR R11	return
0000188C				1118+RE20	DS OF	expected 16 byte result
0000188C				1119+	DROP R5	
0000188C	5263FFFF 00000000			1120	DC XL16' 5263FFFF000000004CFFFFFFFFFFFF9C00'	
00001894	4CFFFFFFFF FFFF9C00					
0000189C	00000000 00018446			1121	DC XL16' 0000000000018446744073709551615C'	
000018A4	74407370 9551615C					
				1122		
				1123 * 9009000000018446744073709551615		
				1124	VRR_B VSCSHP, 3	
000018B0				1125+	DS OFD	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
000018B0		000018B0		1126+	USING *,R5 base for test data and test routine
000018B0	000018CC			1127+T21	DC A(X21) address of test routine
000018B4	0015			1128+	DC H' 21' test number
000018B6	00			1129+	DC X' 00'
000018B7	03			1130+V3_21	DC HL1' 3' scale
000018B8	000018FC			1131+V2_21	DC A(RE21+16) address of v2: 16-byte packed decimal
000018BC	E5E2C3E2 C8D74040			1132+	DC CL8' VSCSHP' instruction name
000018C4	00000010			1133+	DC A(16) result length
000018C8	000018EC			1134+	DC A(RE21) address of expected result
				1135+*	
000018CC				1136+X21	DS 0F
000018CC	E710 8EFC 0006		000010FC	1137+	VL V1, V1FUDGE fudge V1
000018D2	E320 5008 0014		000018B8	1138+	LGF R2, V2_21 get v2
000018D8	E722 0000 0006		00000000	1139+	VL V2, 0(R2)
000018DE	E730 5007 7000		000018B7	1140+	VLEB V3, V3_21, 7 get v3 scale
000018E4	E612 3000 007C			1141+	VSCSHP V1, V2, V3 test instruction
000018EA	07FB			1142+	BR R11 return
000018EC				1143+RE21	DS 0F expected 16 byte result
000018EC				1144+	DROP R5
000018EC	5D1BC2D9 00000000			1145	DC XL16' 5D1BC2D900000000056FA816778E89096'
000018F4	56FA8167 78E89096				
000018FC	90090000 00018446			1146	DC XL16' 90090000000018446744073709551615C'
00001904	74407370 9551615C				
				1147	
				1148 *	99999999990018446744073709551615
				1149	VRR_B VSCSHP, 3
00001910		00001910		1150+	DS 0FD
00001910				1151+	USING *,R5 base for test data and test routine
00001910	0000192C			1152+T22	DC A(X22) address of test routine
00001914	0016			1153+	DC H' 22' test number
00001916	00			1154+	DC X' 00'
00001917	03			1155+V3_22	DC HL1' 3' scale
00001918	0000195C			1156+V2_22	DC A(RE22+16) address of v2: 16-byte packed decimal
0000191C	E5E2C3E2 C8D74040			1157+	DC CL8' VSCSHP' instruction name
00001924	00000010			1158+	DC A(16) result length
00001928	0000194C			1159+	DC A(RE22) address of expected result
				1160+*	
0000192C				1161+X22	DS 0F
0000192C	E710 8EFC 0006		000010FC	1162+	VL V1, V1FUDGE fudge V1
00001932	E320 5008 0014		00001918	1163+	LGF R2, V2_22 get v2
00001938	E722 0000 0006		00000000	1164+	VL V2, 0(R2)
0000193E	E730 5007 7000		00001917	1165+	VLEB V3, V3_22, 7 get v3 scale
00001944	E612 3000 007C			1166+	VSCSHP V1, V2, V3 test instruction
0000194A	07FB			1167+	BR R11 return
0000194C				1168+RE22	DS 0F expected 16 byte result
0000194C				1169+	DROP R5
0000194C	5D1ED09B 00000000			1170	DC XL16' 5D1ED09B00000000057EA5461321798D1'
00001954	57EA5461 321798D1				
0000195C	99999999 90018446			1171	DC XL16' 99999999990018446744073709551615C'
00001964	74407370 9551615C				
				1172	
				1173	
0000196C	00000000			1174	DC F' 0' END OF TABLE
00001970	00000000			1175	DC F' 0'
				1176 *	
				1177 *	table of pointers to individual tests





LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				1211	*****		
				1212	* Register equates		
				1213	*****		
		00000000	00000001	1215 R0	EQU	0	
		00000001	00000001	1216 R1	EQU	1	
		00000002	00000001	1217 R2	EQU	2	
		00000003	00000001	1218 R3	EQU	3	
		00000004	00000001	1219 R4	EQU	4	
		00000005	00000001	1220 R5	EQU	5	
		00000006	00000001	1221 R6	EQU	6	
		00000007	00000001	1222 R7	EQU	7	
		00000008	00000001	1223 R8	EQU	8	
		00000009	00000001	1224 R9	EQU	9	
		0000000A	00000001	1225 R10	EQU	10	
		0000000B	00000001	1226 R11	EQU	11	
		0000000C	00000001	1227 R12	EQU	12	
		0000000D	00000001	1228 R13	EQU	13	
		0000000E	00000001	1229 R14	EQU	14	
		0000000F	00000001	1230 R15	EQU	15	
				1232	*****		
				1233	* Register equates		
				1234	*****		
		00000000	00000001	1236 FPR0	EQU	0	
		00000001	00000001	1237 FPR1	EQU	1	
		00000002	00000001	1238 FPR2	EQU	2	
		00000003	00000001	1239 FPR3	EQU	3	
		00000004	00000001	1240 FPR4	EQU	4	
		00000005	00000001	1241 FPR5	EQU	5	
		00000006	00000001	1242 FPR6	EQU	6	
		00000007	00000001	1243 FPR7	EQU	7	
		00000008	00000001	1244 FPR8	EQU	8	
		00000009	00000001	1245 FPR9	EQU	9	
		0000000A	00000001	1246 FPR10	EQU	10	
		0000000B	00000001	1247 FPR11	EQU	11	
		0000000C	00000001	1248 FPR12	EQU	12	
		0000000D	00000001	1249 FPR13	EQU	13	
		0000000E	00000001	1250 FPR14	EQU	14	
		0000000F	00000001	1251 FPR15	EQU	15	
				1253	*****		
				1254	* Register equates		
				1255	*****		
		00000000	00000001	1257 V0	EQU	0	
		00000001	00000001	1258 V1	EQU	1	
		00000002	00000001	1259 V2	EQU	2	
		00000003	00000001	1260 V3	EQU	3	
		00000004	00000001	1261 V4	EQU	4	



SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES														
BEGIN	I	00000200	2	164	129	160	161	162											
CTLRO	F	0000058C	4	436	174	175	176	177											
DECNUM	C	000010BB	16	507	284	286	293	295	319	321	328	330							
E6TEST	4	00000000	28	524	224														
E6TESTS	F	00001974	4	1179	217														
EDIT	X	0000108F	18	502	285	294	320	329											
ENDTEST	U	00000462	1	350	222														
E0J	I	00000570	4	426	209	353													
E0JPSW	D	00000560	8	424	426														
FAILCONT	U	00000452	1	340															
FAILED	F	00001000	4	466	342	351													
FAILMSG	U	00000408	1	317	238														
FAILPSW	D	00000578	8	428	430														
FAILTEST	I	00000588	4	430	354														
FB0001	F	000002A0	8	193	197	198	200												
FPRO	U	00000000	1	1236															
FPR1	U	00000001	1	1237															
FPR10	U	0000000A	1	1246															
FPR11	U	0000000B	1	1247															
FPR12	U	0000000C	1	1248															
FPR13	U	0000000D	1	1249															
FPR14	U	0000000E	1	1250															
FPR15	U	0000000F	1	1251															
FPR2	U	00000002	1	1238															
FPR3	U	00000003	1	1239															
FPR4	U	00000004	1	1240	265	273	275												
FPR5	U	00000005	1	1241															
FPR6	U	00000006	1	1242															
FPR7	U	00000007	1	1243															
FPR8	U	00000008	1	1244															
FPR9	U	00000009	1	1245															
IMAGE	1	00000000	6620	0															
K	U	00000400	1	450	451	452	453												
K64	U	00010000	1	452															
MB	U	00100000	1	453															
MSG	I	000004A8	4	386	208	369													
MSGCMD	C	000004F6	9	416	399	400													
MSGMSG	C	000004FF	95	417	393	414	391												
MSGMVC	I	000004F0	6	414	397														
MSGOK	I	000004BE	2	395	392														
MSGRET	I	000004DE	4	410	403	406													
MSGSAVE	F	000004E4	4	413	389	410													
NEXTE6	U	000002F4	1	219	241	345													
OPNAME	C	0000000C	8	530	289	324													
PAGE	U	00001000	1	451															
PRT3	C	000010A5	18	505	285	286	287	294	295	296	320	321	322	329	330	331			
PRTLNE	C	00001008	13	475	482	334													
PRTLNG	U	00000040	1	482	333														
PRTNAME	C	00001030	8	478	324														
PRTNUM	C	00001015	3	476	322														
PRTSCALE	C	00001044	3	480	331														
R0	U	00000000	1	1215	123	174	177	197	199	200	201	206	226	227	257	265	274		
					299	333	341	342	368	370	386	389	391	393	395	410			
R1	U	00000001	1	1216	207	236	237	273	274	300	334	351	352	400	414				
R10	U	0000000A	1	1225	162	171	172												
R11	U	0000000B	1	1226	229	230	644	668	692	716	741	766	791	816	841	866	891		















DESC	SYMBOL	SIZE	POS	ADDR
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Entry: 0

Image Region CSECT	IMAGE	6620	0000-19DB	0000-19DB
		6620	0000-19DB	0000-19DB
	ZVE6TST	6620	0000-19DB	0000-19DB

STMT	FILE NAME
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1	/home/tn529/sharedvfp/tests/zvector-e6-18-VSCSHP.asm
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**\*\* NO ERRORS FOUND \*\***